Welcome to DialogClassic Web(tm)

```
 Dialog level 05.02.01D
Last logoff:  06may05 07:17:35
Logon file405 09may05 12:23:26
          *** ANNOUNCEMENT ***
                    ***
--Important Notice to Freelance Authors--
See HELP FREELANCE for more information
                    ***
NEW FILES RELEASED
***FDAnews (File 182)
***German Patents Fulltext (File 324)

***Beilstein Abstracts (File 393)
***Beilstein Facts (File 390)
***Beilstein Reactions (File 391)
                    ***
RELOADED
***Medline (Files 154 & 155)
***ToxFile (File 156)

RESUMED UPDATING
***Canadian Business and Current Affairs (262)
***CorpTech (559)
                    ***
REMOVED                        *** DIALOG HOMEBASE(SM) Main Menu ***

 Information:
  1.  Announcements (new files, reloads, etc.)
  2.  Database, Rates, & Command Descriptions
  3.  Help in Choosing Databases for Your Topic
  4.  Customer Services (telephone assistance, training, seminars, etc.)
  5.  Product Descriptions

 Connections:
  6.  DIALOG(R) Document Delivery
  7.  Data Star(R)

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      /H = Help            /L = Logoff          /NOMENU = Command Mode


Enter an option number to view information or to connect to an online
 service.  Enter a BEGIN command plus a file number to search a database
(e.g., B1 for ERIC).
?

B 2, 3, 4
>>>           4 is temporarily unavailable
>>>1 of the specified files is not available
       09may05 12:24:30 User222506 Session D26.1
             $0.00    0.321 DialUnits FileHomeBase
     $0.00  Estimated cost FileHomeBase
     $0.53  INTERNET
     $0.53  Estimated cost this search
     $0.53  Estimated total session cost   0.321 DialUnits

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2005/Apr W4
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10/693,175

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         (c) 2005 Institution of Electrical Engineers
  File   3:INSPEC 1969-1982
         (c) 1993 Institution of Electrical Engineers

      Set  Items  Description
      ---  -----  -----------
?

S (COMPUTER? OR DATABASE? OR PROCESSOR? OR TERMINAL?) (W) SYNCHRONIZ?
         1001226  COMPUTER?
          142695  DATABASE?
          126078  PROCESSOR?
           93009  TERMINAL?
           43575  SYNCHRONIZ?
      S1     143  (COMPUTER? OR DATABASE? OR PROCESSOR? OR TERMINAL?) (W)
                  SYNCHRONIZ?
?

S S1 AND CONVERT? OR CONVERS?
             143  S1
          183508  CONVERT?
          171196  CONVERS?
      S2  171202  S1 AND CONVERT? OR CONVERS?
?

S S1 AND (CONVERT? OR CONVERS?)
             143  S1
          183508  CONVERT?
          171196  CONVERS?
      S3      6  S1 AND (CONVERT? OR CONVERS?)
?

T S3/FULL/1-6

  3/9/1     (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
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6798768   INSPEC Abstract Number: A2001-03-2852-045, B2001-02-7210G-017,
C2001-02-7470-027
  Title: Real time processor in JT-60 data processing system
  Author(s): Sakata, S.; Koiwa, M.; Aoyagi, T.; Matsuda, T.
  Author Affiliation: Naka Fusion Res. Establ., JAERI, Ibaraki, Japan
  Journal: Fusion Engineering and Design Conference Title: Fusion Eng. Des.
(Switzerland)    vol.48, no.1-2    p.225-30
  Publisher: Elsevier,
  Publication Date: Aug. 2000  Country of Publication: Switzerland
  CODEN: FEDEEE  ISSN: 0920-3796
  SICI: 0920-3796(200008)48:1/2L.225:RTPD;1-E
  Material Identity Number: F111-2000-004
  U.S. Copyright Clearance Center Code: 0920-3796/2000/$20.00
  Conference Title: 2nd IAEA Technical Committee Meeting on Control Data
Acquisition and Remote Participation on Fusion Research
  Conference Date: 19-21 July 1999    Conference Location: Lisbon, Portugal
  Document Number: S0920-3796(00)00134-4
  Language: English    Document Type: Conference Paper (PA); Journal Paper
(JP)
  Treatment: Experimental (X); Practical (P)
  Abstract: Real time processor, RTP, is a basic subsystem in the JT-60
data processing system and plays an important role in JT-60 feedback
```

control utilizing various diagnostic signals. An original mini-computer system was replaced in 1994 with a workstation. It has 2 CPU's with a real-time parallel UNIX. During the experiment, one CPU communicates with the main computer synchronized with the experimental sequence, and the other executes a real-time process with 1 ms clock. RTP has been upgraded to a compatible RISC workstation with a faster A/D converter in 1997 in response to increased requests of handling the increased signals in more complicated manners. After this upgrade, an elapsed time is reduced to ~75% and an I/O time is now dominant. To reduce a CAMAC access time, we try to use a reflective memory for the data transfer. Now RTP handles six kinds of signals to control an electron density, a neutron emission, an electron density and a radiation in the divertor region, and a neutral pressure. RTP will handle five more kinds of signals this year and be used for an advanced control with more complicated processing. (9 Refs)

Subfile: A B C

Descriptors: CAMAC; data acquisition; data analysis; fusion reactor instrumentation; nuclear engineering computing; real-time systems; SCADA systems; Tokamak devices; Unix

Identifiers: real time processor; JT-60 tokamak; data processing system; feedback control; plasma diagnostics; real-time parallel UNIX; RISC workstation; AD converter; data handling; CAMAC access time; reflective memory; data transfer; machine control; advanced control

Class Codes: A2852L (Fusion reactor instrumentation); A0650D (Data gathering, processing, and recording, data displays including digital techniques); B7210G (Data acquisition systems); C7470 (Nuclear engineering computing); C5520 (Data acquisition equipment and techniques); C3210G (Data acquisition systems for control); C6130 (Data handling techniques); C7320 (Physics and chemistry computing)

3/9/2 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

5953391 INSPEC Abstract Number: C9808-4240P-003

Title: Self-stabilization with global rooted synchronizers

Author(s): Alima, L.O.; Beauquier, J.; Datta, A.K.; Tixeuil, S.

Author Affiliation: Unite d'Inf., Univ. Catholique de Louvain, Belgium

Conference Title: Proceedings. 18th International Conference on Distributed Computing Systems (Cat. No.98CB36183) p.102-9

Editor(s): Papazoglou, M.P.; Takizawa, M.; Kramer, B.; Chanson, S.

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1998 Country of Publication: USA xviii+631 pp.

ISBN: 0 8186 8292 2 Material Identity Number: XX98-01360

U.S. Copyright Clearance Center Code: 0 8186 8292 2/98/$10.00

Conference Title: Proceedings of 18th International Conference on Distributed Computing Systems

Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Distributed Process

Conference Date: 26-29 May 1998 Conference Location: Amsterdam, Netherlands

Language: English Document Type: Conference Paper (PA)

Treatment: Theoretical (T)

Abstract: We propose a self-stabilizing synchronization technique, called the global rooted synchronization, that synchronizes processors in a tree network. This synchronizer converts a synchronous protocol for tree networks into a self-stabilizing version. The synchronizer requires only O(1) memory (other than the memory needed to maintain the tree) at each node regardless of the size of the network, stabilizes in O(h) time, where

h is the height of the tree, and does not invoice any global operations. Applications of this technique are presented. (19 Refs)
Subfile: C
Descriptors: distributed algorithms; software fault tolerance; synchronisation; trees (mathematics)
Identifiers: self-stabilizing synchronization; global rooted synchronization; processor synchronization; tree network; synchronous protocol; memory; global operations; distributed algorithms
Class Codes: C4240P (Parallel programming and algorithm theory); C6150N (Distributed systems software); C1160 (Combinatorial mathematics)

3/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5613048 INSPEC Abstract Number: B9708-6140-046, C9708-5260-006
Title: Optimizing synchronization in multiprocessor DSP systems
Author(s): Bhattacharyya, S.S.; Sriram, S.; Lee, E.A.
Author Affiliation: Semicond. Res. Lab., Hitachi America Ltd., San Jose, CA, USA
Journal: IEEE Transactions on Signal Processing vol.45, no.6 p. 1605-18
Publisher: IEEE,
Publication Date: June 1997 Country of Publication: USA
CODEN: ITPRED ISSN: 1053-587X
SICI: 1053-587X(199706)45:6L.1605:OSMS;1-4
Material Identity Number: 0649-97007
U.S. Copyright Clearance Center Code: 1053-587X/97/$10.00
Document Number: S1053-587X(97)04211-6
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: This paper is concerned with multiprocessor implementations of embedded applications specified as iterative dataflow programs in which synchronization overhead can be significant. We develop techniques to alleviate this overhead by determining a minimal set of processor synchronizations that are essential for correct execution. Our study is based in the context of self-timed execution of iterative dataflow programs. An iterative dataflow program consists of a dataflow representation of the body of a loop that is to be iterated an indefinite number of times; dataflow programming in this form has been studied and applied extensively, particularly in the context of signal processing software. Self-timed execution refers to a combined compile-time/run-time scheduling strategy in which processors synchronize with one another based only on interprocessor communication requirements, and thus, synchronization of processors at the end of each loop iteration does not generally occur. We introduce a new graph-theoretic framework based on a data structure called the synchronization graph for analyzing and optimizing synchronization overhead in self-timed, iterative dataflow programs. We show that the comprehensive techniques that have been developed for removing redundant synchronizations in noniterative programs can be extended in this framework to optimally remove redundant synchronizations in our context. We also present an optimization that converts a feedforward dataflow graph into a strongly connected graph in such a way as to reduce synchronization overhead without slowing down execution. (30 Refs)
Subfile: B C
Descriptors: data flow computing; data flow graphs; feedforward; graph theory; iterative methods; multiprocessing systems; optimisation; processor

scheduling; signal processing; synchronisation
Identifiers: multiprocessor DSP systems; iterative data flow programs; synchronization overhead reduction; processor synchronization; self-timed execution; iterative dataflow programs; dataflow representation; dataflow programming; signal processing software; compile-time/run-time scheduling; interprocessor communication requirements; graph-theoretic framework; data structure; synchronization graph; redundant synchronization removal; noniterative programs; feedforward dataflow graph; strongly connected graph
Class Codes: B6140 (Signal processing and detection); B0260 (Optimisation techniques); C5260 (Digital signal processing); C5440 (Multiprocessing systems); C1180 (Optimisation techniques); C4240P (Parallel programming and algorithm theory)

3/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5065478 INSPEC Abstract Number: C9511-5440-026
Title: Minimizing synchronization overhead in statically scheduled multiprocessor systems
Author(s): Bhattacharyya, S.S.; Sriram, S.; Lee, E.A.
Author Affiliation: Semicond. Res. Lab., Hitachi America Ltd., San Jose, CA, USA
Conference Title: Proceedings. The International Conference on Application Specific Array Processors (Cat. No.95TB8098) p.298-309
Editor(s): Cappello, P.; Mongenet, C.; Perrin, G.-R.; Quinton, P.; Robert, Y.
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1995 Country of Publication: USA xiii+340 pp.
ISBN: 0 8186 7109 2
U.S. Copyright Clearance Center Code: 1063 6862/95/$4.00
Conference Title: Proceedings The International Conference on Application Specific Array Processors
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on VLSI
Conference Date: 24-26 July 1995 Conference Location: Strasbourg, France
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Synchronization overhead can significantly degrade performance in embedded multiprocessor systems. This paper develops techniques to determine a minimal set of processor synchronizations that are essential for correct execution in an embedded multiprocessor implementation. Our study is based in the context of self-timed execution of iterative dataflow programs; dataflow programming in this form has been applied extensively, particularly in the context of signal processing software. Self-timed execution refers to a combined compile-time/run-time scheduling strategy in which processors synchronize with one another only based on inter-processor communication requirements, and thus, synchronization of processors at the end of each loop iteration does not generally occur. We introduce a new graph-theoretic framework, based on a data structure called the synchronization graph, for analyzing and optimizing synchronization overhead in self-timed, iterative dataflow programs. We also present an optimization that involves converting a synchronization graph that is not strongly connected into a strongly connected graph. (17 Refs)
Subfile: C
Descriptors: multiprocessing systems; processor scheduling; synchronisation
Identifiers: synchronization overhead; statically scheduled

multiprocessor systems; embedded multiprocessor; iterative dataflow programs; dataflow programming; graph-theoretic framework; data structure; synchronization graph
Class Codes: C5440 (Multiprocessing systems); C6150N (Distributed systems software)

3/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

03491018 INSPEC Abstract Number: C89067933
Title: Implementing a Scheme-based parallel processing system
Author(s): Miller, J.S.
Author Affiliation: Dept. of Comput. Sci., Brandeis Univ., Waltham, MA, USA
Journal: International Journal of Parallel Programming vol.17, no.5 p.367-402
Publication Date: Oct. 1988 Country of Publication: USA
CODEN: IJPPE5 ISSN: 0885-7458
U.S. Copyright Clearance Center Code: 0885-7458/88/1000-0367$06.00/0
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The Scheme language can be converted into a parallel processing language by adding two new data types, two processor synchronization primitives, and a task distribution mechanism. The mechanisms that support task creation, scheduling, and task synchronization are built using these extensions and features already present in the sequential language. Implementing the core of the parallel processing component in Scheme itself provides a testbed for a variety of experiments and extensions. MultiScheme is the system resulting from these extensions. The author describes the Scheme procedures, collectively referred to as the scheduler, that implement the critical operations of MultiScheme. The system supports the future construct derived from R. Halstead's Multilisp (1985) as the simple model for parallelism. (13 Refs)
Subfile: C
Descriptors: LISP listings; parallel programming; programming environments; scheduling; synchronisation
Identifiers: Scheme-based parallel processing system; Scheme language; parallel processing language; data types; processor synchronization primitives; task distribution mechanism; task creation; scheduling; task synchronization; sequential language; parallel processing; Scheme; testbed; MultiScheme; Scheme procedures; scheduler; future construct; Multilisp; simple model
Class Codes: C6115 (Programming support); C6150 (Systems software); C6110 (Systems analysis and programming)

3/9/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02725052 INSPEC Abstract Number: A86098256, C86043063
Title: Personal computer-based measurement and control system for spectroscopy
Author(s): Matsuura, K.; Yutani, T.; Nakajima, T.; Kishida, S.; Tsurumi, I.; Yamada, T.
Author Affiliation: Dept. of Electron., Fac. of Eng., Tottori Univ., Japan

```
  Journal: Journal of the Spectroscopical Society of Japan    vol.34, no.6
p.371-6
  Publication Date: 1985  Country of Publication: Japan
  CODEN: BUKKAT  ISSN: 0038-7002
  Language: Japanese    Document Type: Journal Paper (JP)
  Treatment: Applications (A); Practical (P)
  Abstract: A number of studies have been made on computer-aided control
and instrumentation and trial development of the related circuits. The
authors have developed a multi-purpose control/instrumentation system for
spectroscopic experiments by using two kinds of general-purpose 8-bit
personal computers. The system is composed of: CTC (Counter and Timer
Circuit) with functions of computer synchronization with external
equipment, periodical pulse generation, pulse counting, etc.; A/D and D/A
converter units; and PIO (Parallel Input/Output port unit) for digital
signal input/output operation. Simple data processing and printing are
carried out by the computer equipped with CRT, printer and mini-floppy
disk, and complicated data processing is done by the host computer. (18
 Refs)
  Subfile: A C
  Descriptors: computerised spectroscopy; microcomputer applications
  Identifiers: A/D converter; D/A converter; parallel input-output port
unit; counter and timer circuit; spectroscopy; computer-aided control;
instrumentation; 8-bit personal computers; CTC; computer synchronization;
periodical pulse generation; digital signal; CRT; printer; mini-floppy disk
; data processing
  Class Codes: A0650  (Data handling and computation); A0765  (Optical
spectroscopy and spectrometers); C3380D (Physical instruments); C7320  (
Physics and Chemistry)
?

B 8, 208
       09may05 12:27:30 User222506 Session D26.2
            $5.02    0.609 DialUnits File2
              $17.40  6 Type(s) in Format  9
           $17.40  6 Types
    $22.42  Estimated cost File2
            $1.36    0.165 DialUnits File3
     $1.36  Estimated cost File3
            OneSearch, 2 files,  0.773 DialUnits FileOS
     $1.06  INTERNET
    $24.84  Estimated cost this search
    $25.37  Estimated total session cost   1.095 DialUnits

SYSTEM:OS  - DIALOG OneSearch
  File   8:Ei Compendex(R) 1970-2005/May W1
         (c) 2005 Elsevier Eng.  Info. Inc.
  File 208:ONTAP(R) Ei Compendex(R)
         (c) 1997 Elsevier Eng. Info. Inc.

      Set  Items  Description
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S (COMPUTER? OR DATABASE? OR PROCESSOR? OR TERMINAL?) (W) SYNCHRONIZ?
         1041497  COMPUTER?
           87802  DATABASE?
           66124  PROCESSOR?
           55231  TERMINAL?
           30712  SYNCHRONIZ?
      S1     220  (COMPUTER? OR DATABASE? OR PROCESSOR? OR TERMINAL?) (W)
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                SYNCHRONIZ?
?

S S1 AND (CONVERT? OR CONVERS?)
             220  S1
          110669  CONVERT?
          124234  CONVERS?
      S2      11  S1 AND (CONVERT? OR CONVERS?)
?

S S2 AND PDA
              11  S2
            2009  PDA
      S3       0  S2 AND PDA
?

S S2 AND (ELECTRONIC (W) MAIL)
              11  S2
          232690  ELECTRONIC
            8211  MAIL
            5764  ELECTRONIC(W)MAIL
      S4       0  S2 AND (ELECTRONIC (W) MAIL)
?

S S1 AND PDA
             220  S1
            2009  PDA
      S5       2  S1 AND PDA
?

S S1 AND (ELECTRONIC ADJ1 MAIL)
             220  S1
               0  ELECTRONIC ADJ1 MAIL
      S6       0  S1 AND (ELECTRONIC ADJ1 MAIL)
?

T S5/FULL/1-2

  5/9/1     (Item 1 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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06127037   E.I. No: EIP02377076661
   Title:   Fast   PDA synchronization using characteristic polynomial
 interpolation
  Author: Trachtenberg, Ari; Starobinski, David; Agarwal, Sachin
  Corporate Source: Dept. of Elec. and Comp. Engineering Boston University,
Boston, MA,  United States
  Conference Title: IEEE Infocom 2002
  Conference  Location:  New  York,  NY,  United  States   Conference Date:
20020623-20020627
  Sponsor: IEEE
  E.I. Conference No.: 59460
  Source:  Proceedings  -  IEEE  INFOCOM  v 3 2002. p 1510-1519 (IEEE cat n
02ch37364)
  Publication Year: 2002
  CODEN: PINFEZ   ISSN: 0743-166X
  Language: English
  Document Type: CA; (Conference Article)   Treatment: A; (Applications)
  Journal Announcement: 0209W3
```

Abstract: Modern Personal Digital Assistant (PDA) architectures often utilize a wholesale data transfer protocol known as "slow sync" for synchronizing PDAs with Personal Computers (PCs). This approach is markedly inefficient with respect to bandwidth usage and latency, since the PDA and PC typically share many common records. We propose, analyze, and implement a novel PDA synchronization scheme (CPIsync) predicated upon recent information-theoretic research. The salient property of this scheme is that its communication complexity depends on the number of differences between the PDA and PC, and is essentially independent of the overall number of records. Moreover, our implementation shows that the computational complexity of CPIsync is practical, and that the overall latency is typically much smaller than that of slow sync. Thus, CPIsync has potential for significantly improving synchronization protocols for PDAs and, more generally, for heterogeneous networks of many machines. 33 Refs.

Descriptors: *Personal digital assistants; Polynomials; Interpolation; Personal computers; Synchronization; Computational complexity; Computer architecture

Identifiers: Handheld devices; Characteristic polynomial

Classification Codes:

723.5 (Computer Applications); 921.1 (Algebra); 722.4 (Digital Computers & Systems); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))

723 (Computer Software, Data Handling & Applications); 921 (Applied Mathematics); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

5/9/2 (Item 2 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

05804635 E.I. No: EIP00025069884

Title: Linking and messaging from real paper in the paper PDA

Author: Heiner, Jeremy M.; Hudson, Scott E.; Tanaka, Kenichiro

Corporate Source: Carnegie Mellon Univ, Pittsburgh, PA, USA

Conference Title: Proceedings of the 1999 12th Annual ACM Symposium on User Interface Software and Technology (UIST '99)

Conference Location: Ashville, NC, USA Conference Date: 20991107-20991110

Sponsor: ACM

E.I. Conference No.: 56090

Source: UIST (User Interface Software and Technology): Proceedings of the ACM Symposium v 1 n 1 1999. ACM, New York, NY, USA. p 179-186

Publication Year: 1999

CODEN: UISTFM

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); G ; (General Review)

Journal Announcement: 0104W3

Abstract: It is well known that paper is a very fluid, natural, and easy to use medium for manipulating some kinds of information. It is familiar, portable, flexible, inexpensive, and offers good readability properties. Paper also has well known limitations when compared with electronic media. Work in hybrid paper electronic interfaces seeks to bring electronic capabilities to real paper in order to obtain the best properties of each. This paper describes a hybrid paper electronic system - the Paper PDA- which is designed to allow electronic capabilities to be employed within a conventional paper notebook, calendar, or organizer. The Paper PDA is based on a simple observation: a paper notebook can be synchronized with a body

of electronic information much like an electronic PDA can be synchronized with information hosted on a personal computer. This can be accomplished by scanning, recognizing and processing its contents, then printing a new copy. This paper introduces the Paper PDA concept and considers interaction techniques and applications designed to work within the Paper PDA. The StickerLink technique supports on-paper hyperlinking using removable paper stickers. Two applications are also considered which look at aspects of electronic communications via the Paper PDA. (Author abstract) 15 Refs.
Descriptors: *Interactive computer systems; Data communication systems; Hybrid computers; Synchronization; Personal computers; Scanning; User interfaces; Human computer interaction
Identifiers: Hybrid paper electronic interfaces; Personal digital assistants; Stickerlink technique; Hyperlinking
Classification Codes:
722.4 (Digital Computers & Systems); 722.3 (Data Communication, Equipment & Techniques); 722.5 (Analog & Hybrid Computers); 741.3 (Optical Devices & Systems); 722.2 (Computer Peripheral Equipment)
722 (Computer Hardware); 741 (Optics & Optical Devices)
72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY)
?

T S2/FULL/1-11

2/9/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

07327831 E.I. No: EIP05149019540
Title: A relational database for the monitoring and analysis of watershed hydrologic functions: I. Database design and pertinent queries
Author: Carleton, Christian J.; Dahlgren, Randy A.; Tate, Kenneth W.
Corporate Source: Dept. of Land, Air/Water Resources University of California, Davis, CA 95616, United States
Source: Computers and Geosciences v 31 n 4 May 2005. p 393-402
Publication Year: 2005
CODEN: CGEODT ISSN: 0098-3004
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0504W2
Abstract: The need to monitor water quantity and quality has increased dramatically in recent years due to total maximum daily load requirements that address non-point source pollutants in our nation's water bodies. This has resulted in the need for data management techniques and tools to manage the vast amount of new hydrologic data being collected. Data must be stored, checked for errors, manipulated, retrieved for analysis, and shared within the hydrologic community. The Watershed Monitoring and Analysis Database is a relational database application developed as a data management tool to efficiently and accurately address the needs of individuals and groups responsible for maintaining hydrologic data sets. Stream flow, water quality, and meteorological data can be stored and manipulated within the database. Both remedial and advanced tasks can be simplified with the help of the user interface application, such as quality assurance/quality control (QA/QC) calculations, application of correction and conversion factors, retrieval of desired data for advanced analysis, and data comparisons among multiple study sites. Web integration and local area network (LAN) database synchronization can be supported depending upon the database engine used. The objectives of this paper are to: (1) present in detail the database architecture, including table structures and overall database design, and (2) provide useful queries to retrieve data that involve calculations, comparisons, and basic QA/QC

protocols. Developed using Microsoft Access, the concepts and strategies covered in this paper may be applied to any commercially available relational database. copy 2004 Elsevier Ltd. All rights reserved. 10 Refs.
Descriptors: *Watersheds; Hydrology; Relational database systems; Monitoring; Water quality; Pollution; Meteorology; Numerical methods; Data acquisition; Local area networks
Identifiers: Watershed hydrological functions; Data management techniques ; Non-point source pollutants
Classification Codes:
444.1 (Surface Water); 723.3 (Database Systems); 445.2 (Water Analysis); 454.2 (Environmental Impact & Protection); 921.6 (Numerical Methods); 723.2 (Data Processing)
444 (Water Resources); 723 (Computer Software, Data Handling & Applications); 445 (Water Treatment); 454 (Environmental Engineering); 443 (Meteorology); 921 (Applied Mathematics)
44 (WATER & WATERWORKS ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 45 (POLLUTION, SANITARY ENGINEERING & WASTES); 92 (ENGINEERING MATHEMATICS)

2/9/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

07223301 E.I. No: EIP05038791647
Title: Autonomous virtual human research for dialog system
Author: Sugiyama, Saori; Abe, Norihiro; Tanaka, Kazuaki; Taki, Hiroaki; Yagi, Tetsuya
Corporate Source: Kyushu Institute of Technology Graduate School, Iizuka, Fukuoka 820-8502, Japan
Conference Title: 2004 IEEE Conference on Cybernetics and Intelligent Systems
Conference Location: Singapore Conference Date: 20041201-20041203
Sponsor: Institute of Electrical and Electronics Engineers, IEEE; IEEE SMC Society Singapore Chapter; IEEE R and A Society Singapore Chapter
E.I. Conference No.: 64160
Source: 2004 IEEE Conference on Cybernetics and Intelligent Systems 2004 IEEE Conference on Cybernetics and Intelligent Systems 2004. (IEEE cat n 04ex912c)
Publication Year: 2004
ISBN: 0780386442
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 0501W4
Abstract: With the development of data processing technology, the number of people using a computer is rapidly growing now. And they came to use it in the everyday life of ordinary homes. However, it is hard for elderly people and disabled persons to treat an interface device such as a mouse and a keyboard. For this reason, the dialog system is needed that permits them to dialog with a computer. A virtual human called avatar is introduced into virtual space. Users can talk to him as if he talked to a real person. When a man talks in real space, the partner chimes in according to a speaker's utterance. By synchronizing utterance with a behavior, a partner can understand a speaker's intention correctly. Moreover, relation between a listener and a speaker is not always fixed in man's conversation, and the relation interchanges. This research proposes how to understand the conversation accompanied with the pointing behavior. 9 Refs.
Descriptors: *Data processing; Interfaces (computer); Synchronization;

Communication systems; Speech; Computer vision; Approximation theory
Identifiers: Avatar; Virtual human; Conversation; Dialog system
Classification Codes:
723.2 (Data Processing); 722.2 (Computer Peripheral Equipment); 731.1 (Control Systems); 751.5 (Speech); 723.5 (Computer Applications); 741.2 (Vision); 921.6 (Numerical Methods)
723 (Computer Software, Data Handling & Applications); 722 (Computer Hardware); 731 (Automatic Control Principles & Applications); 716 (Electronic Equipment, Radar, Radio & Television); 751 (Acoustics, Noise & Sound); 741 (Light, Optics & Optical Devices); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 75 (SOUND & ACOUSTICAL TECHNOLOGY); 74 (LIGHT & OPTICAL TECHNOLOGY); 92 (ENGINEERING MATHEMATICS)

2/9/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06984666 E.I. No: EIP04348316744
Title: Implementing sequentially consistent programs on processor consistent platforms
Author: Higham, Lisa; Kawash, Jalal
Corporate Source: Department of Computer Science University of Calgary, Calgary, Alta., Canada
Conference Title: Proceedings on the International Symposium on Parallel Architectures, Algorithms and Networks, I-SPAN
Conference Location: Hong Kong, China Conference Date: 20040510-20040512
Sponsor: University of Hong Kong; Hong Kong Polytechnic University
E.I. Conference No.: 63317
Source: Proceedings of the International Symposium on Parallel Architectures, Algorithms and Networks, I-SPAN Proceedings on the International Symposium on Parallel Architectures, Algorithms and Networks, I-SPAN 2004 2004.
Publication Year: 2004
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0408W4
Abstract: This paper investigates the existence of compilers to convert programs that use shared read/write variables, with sequentially consistent memory semantics, to programs that use read/write variables with the semantics of one variant of processor consistency, known as PC-G. We first provide a simple program transformation, and prove that it compiles any 2-process program with only single-writer variables. We show that this transformation is not a general compiler for 3 or more processes; however, it does correctly transform some specific n-process programs. In particular, for the special case of the (expected) wait-free Test & Set algorithm of Tromp and Vitanyi, our transformation extends to any number of processes. Thus, one notable outcome is an implementation of Test&Set on PC-G that uses only reads and writes of shared variables. This is the first expected wait-free implementation of Test&Set on any weak memory model, and illustrates the use of randomization with a weak memory model. 15 Refs.
Descriptors: *Program compilers; Program processors; Semantics; Data storage equipment; Personal computers; Synchronization; Algorithms; Mathematical models
Identifiers: Memory semantics; Program transformations; Shared memory; Read/write variables

Classification Codes:
723.1 (Computer Programming); 903.2 (Information Dissemination); 722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 731.1 (Control Systems)
723 (Computer Software, Data Handling & Applications); 903 (Information Science); 722 (Computer Hardware); 731 (Automatic Control Principles & Applications); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 90 (ENGINEERING, GENERAL); 73 (CONTROL ENGINEERING); 92 (ENGINEERING MATHEMATICS)

2/9/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05665098 E.I. No: EIP00105350470
Title: Real time processor in JT-60 data processing system
Author: Sakata, S.; Koiwa, M.; Aoyagi, T.; Matsuda, T.
Corporate Source: Japan Atomic Energy Research Inst, Ibaraki, Jpn
Source: Fusion Engineering and Design v 48 n 1 Aug 2000. p 225-230
Publication Year: 2000
CODEN: FEDEEE ISSN: 0920-3796
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 0011W3
Abstract: Real time processor, RTP, is a basic subsystem in the JT-60 data processing system and plays an important role in JT-60 feedback control utilizing various diagnostic signals. An original mini-computer system was replaced in 1994 with a workstation. It has 2 CPU's with a real-time parallel UNIX. During the experiment, one CPU communicates with the main computer synchronized with the experimental sequence, and the other executes a real-time process with 1 ms clock. RTP has been upgraded to a compatible RISC workstation with a faster A/D converter in 1997 in response to increased requests of handling the increased signals in more complicated manners. After this upgrade, an elapsed time is reduced to approximately 75% and an I/O time is now dominant. To reduce a CAMAC access time, we try to use a reflective memory for the data transfer. Now RTP handles six kinds of signals to control an electron density, a neutron emission, an electron density and a radiation in the divertor region, and a neutral pressure. RTP will handle five more kinds of signals this year and be used for an advanced control with more complicated processing. (Author abstract) 9 Refs.
Descriptors: *Data processing; Real time systems; Program processors; Feedback control; Program diagnostics; Parallel processing systems; Computer workstations; UNIX; Reduced instruction set computing; Analog to digital conversion
Identifiers: Real time processors
Classification Codes:
723.2 (Data Processing); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming); 731.1 (Control Systems)
723 (Computer Software); 722 (Computer Hardware); 731 (Automatic Control Principles)
72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING)

2/9/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04930570 E.I. No: EIP98024045472

Title: Low cost Power Factor Correction (PFC) converter using delay control
Author: Lee, K.C.; Cho, B.H.
Corporate Source: Seoul Natl Univ, Seoul, South Korea
Conference Title: Proceedings of the 1997 Power Conversion Conference. Part 1 (of 2)
Conference Location: Nagaoka, Jpn Conference Date: 19970803-19970806
Sponsor: IEE Japan; IEEE
E.I. Conference No.: 47766
Source: PCC - Nagaoka Proceedings of the Power Conversion Conference - Nagaoka, PCC v 1 1997. IEEE, Piscataway, NJ, USA,97TH8266. p 335-340
Publication Year: 1997
CODEN: 002755
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 9804W1
Abstract: A low cost universal input voltage (90 to approximately 264 V) Power Factor Correction (PFC) converter for 200 W power supply in a personal computer (PC) is proposed. it consists of the PFC part followed by a dc-dc converter as in a conventional two-stage scheme. However a single PWM controller is used as in a single-stage, single-switch PFC scheme. The switch in the PFC part is synchronized with the switch in the dc-dc converter and it has a fixed frequency. Employing a simple delay scheme using the pulse and feedback signal of the dc-dc converter, the PFC switch is controlled to limit the capacitor, voltage within a range for the optimum efficiency and cost. A tradeoff study shows that it indeed offers better efficiency and cost reduction compared to single switch approaches for this power level. The design procedure and experimented results are presented. (Author abstract) 5 Refs.
Descriptors: *Power converters; Electric power factor correction; Electric power supplies to apparatus; Pulse width modulation; Electric switches; Capacitors; Cost effectiveness; Feedback; Personal computers; Synchronization
Identifiers: Delay control
Classification Codes:
704.2 (Electric Equipment); 703.1 (Electric Networks); 701.1 (Electricity: Basic Concepts & Phenomena); 704.1 (Electric Components); 911.2 (Industrial Economics)
704 (Electric Components & Equipment); 703 (Electric Circuits); 701 (Electricity & Magnetism); 714 (Electronic Components); 911 (Industrial Economics)
70 (ELECTRICAL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS); 91 (ENGINEERING MANAGEMENT)

2/9/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04726944 E.I. No: EIP97063701155
Title: Optimizing synchronization in multiprocessor DSP systems
Author: Bhattacharyya, Shuvra S.; Sriram, Sundararajan; Lee, Edward A.
Corporate Source: Hitachi America, Ltd, San Jose, CA, USA
Source: IEEE Transactions on Signal Processing v 45 n 6 Jun 1997. p 1605-1618
Publication Year: 1997
CODEN: ITPRED ISSN: 1053-587X
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 9708W2
Abstract: This paper is concerned with multiprocessor implementations of embedded applications specified as iterative dataflow programs in which synchronization overhead can be significant. We develop techniques to alleviate this overhead by determining a minimal set of processor synchronizations that are essential for correct execution. Our study is based in the context of self-timed execution of iterative dataflow programs. An iterative dataflow program consists of a dataflow representation of the body of a loop that is to be iterated an indefinite number of times; dataflow programming in this form has been studied and applied extensively, particularly in the context of signal processing software. Self-timed execution refers to a combined compile-time/run-time scheduling strategy in which processors synchronize with one another based only on interprocessor communication requirements, and thus, synchronization of processors at the end of each loop iteration does not generally occur. We introduce a new graph-theoretic framework based on a data structure called the synchronization graph for analyzing and optimizing synchronization overhead in self-timed, iterative dataflow programs. We show that the comprehensive techniques that have been developed for removing redundant synchronizations in noniterative programs can be extended in this framework to optimally remove redundant synchronizations in our context. We also present an optimization that converts a feedforward dataflow graph into a strongly connected graph in such a way as to reduce synchronization overhead without slowing down execution. (Author abstract) 30 Refs.
Descriptors: *Multiprocessing systems; Synchronization; Optimization; Digital signal processing; Iterative methods; Data structures; Computer software
Identifiers: Iterative dataflow program
Classification Codes:
722.4 (Digital Computers & Systems); 731.1 (Control Systems); 921.5 (Optimization Techniques); 716.1 (Information & Communication Theory); 723.2 (Data Processing); 921.6 (Numerical Methods)
722 (Computer Hardware); 731 (Automatic Control Principles); 921 (Applied Mathematics); 716 (Radar, Radio & TV Electronic Equipment); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING); 92 (ENGINEERING MATHEMATICS); 71 (ELECTRONICS & COMMUNICATIONS)

2/9/7 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04253142 E.I. No: EIP95092855036
Title: Minimizing synchronization overhead in statically scheduled multiprocessor systems
Author: Bhattacharyya, Shuvra S.; Sriram, Sundararajan; Lee, Edward A.
Corporate Source: Hitachi America, Ltd, San Jose, CA, USA
Conference Title: Proceedings of the International Conference on Application Specific Array Processors, ASAP'95
Conference Location: Strasbourg, Fr Conference Date: 19950724-19950726
Sponsor: IEEE
E.I. Conference No.: 43581
Source: Proceedings of the International Conference on Application Specific Array Processors 1995. IEEE, Piscataway, NJ, USA,95TB8098. p 298-309
Publication Year: 1995
CODEN: 85PHAP ISSN: 1063-6862
Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9511W2
Abstract: Synchronization overhead can significantly degrade performance in embedded multiprocessor systems. This paper develops techniques to determine a minimal set of processor synchronizations that are essential for correct execution in an embedded multiprocessor implementation. Our study is based in the context of self-timed execution of iterative dataflow programs; dataflow programming in this form has been applied extensively, particularly in the context of signal processing software. Self-timed execution refers to a combined compile-time/run-time scheduling strategy in which processors synchronize with one another only based on inter-processor communication requirements, and thus, synchronization of processors at the end of each loop iteration does not generally occur. We introduce a new graph-theoretic framework, based on a data structure called the synchronization graph, for analyzing and optimizing synchronization overhead in self-timed, iterative dataflow programs. We also present an optimization that involves converting a synchronization graph that is not strongly connected into a strongly connected graph. (Author abstract) 17 Refs.
Descriptors: *Multiprocessing systems; Synchronization; Computational complexity; Iterative methods; Multiprogramming; Graph theory; Optimization ; Resource allocation
Identifiers: Synchronization overhead; Statically scheduled multiprocessor systems; Self timed execution; Iterative dataflow programs; Synchronization graph
Classification Codes:
722.4 (Digital Computers & Systems); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 921.6 (Numerical Methods); 723.1 (Computer Programming); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 921.5 (Optimization Techniques)
722 (Computer Hardware); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

2/9/8 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04240136 E.I. No: EIP95092838547
Title: Multimodal interaction in human communication
Author: Watanuki, Keiko; Sakamoto, Kenji; Togawa, Fumio
Corporate Source: Sharp Corp, Chiba-shi, Jpn
Source: IEICE Transactions on Information and Systems v E78-D n 6 Jun 1995. p 609-615
Publication Year: 1995
CODEN: ITISEF ISSN: 0916-8532
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review); T; (Theoretical)
Journal Announcement: 9510W5
Abstract: We are developing multimodal man-machine interfaces through which users can communicate by integrating speech, gaze, facial expressions, and gestures such as nodding and finger pointing. Such multimodal interfaces are expected to provide more flexible, natural and productive communications between humans and computers. To achieve this goal, we have taken the approach of modeling human behavior in the context of ordinary face-to-face conversations. As the first step, we have implemented a system which utilizes video and audio recording equipment to

capture verbal and nonverbal information in interpersonal communications. Using this system, we have collected data from a task-oriented conversation between a guest (subject) and a receptionist at company reception desk, and quantitatively analyzed this data with respect to multi-modalities which would be functional in fluid interactions. This paper presents detailed analyses of the data collected: (1) head nodding and eye-contact are related to the beginning and end of speaking turns, acting to supplement speech information; (2) listener responses occur after an average of 0.35 sec. from the receptionist's utterance of a keyword, and turn-taking for tag-questions occurs after an average of 0.44 sec.; and (3) there is a rhythmical coordination between speakers and listeners. (Author abstract) 14 Refs.

Descriptors: *Database systems; Interactive computer systems; Interfaces (computer); Synchronization; Human engineering; Systems analysis

Identifiers: Multimodal interaction; Human communication; Nodding; Eye contact

Classification Codes:

723.3 (Database Systems); 722.4 (Digital Computers & Systems); 722.2 (Computer Peripheral Equipment); 461.4 (Human Engineering)

723 (Computer Software); 722 (Computer Hardware); 461 (Biotechnology)

72 (COMPUTERS & DATA PROCESSING); 46 (BIOENGINEERING)

2/9/9 (Item 9 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

04194477 E.I. No: EIP95031606836

Title: New class of weighting functions readily available with sampled data processors

Author: Ripamonti, G.; Castoldi, A.; Spigarolo, R.; Gatti, E.

Corporate Source: Universita degli Studi di Milano, Milano, Italy

Conference Title: Proceedings of the 1993 IEEE Nuclear Science Symposium & Medical Imaging Conference

Conference Location: San Francisco, CA, USA Conference Date: 19931030-19931106

Sponsor: IEEE

E.I. Conference No.: 20646

Source: IEEE Nuclear Science Symposium & Medical Imaging Conference n pt 1 1994. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 630-634

Publication Year: 1994

CODEN: 85OQAD ISBN: 0-7803-1488-3

Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review)

Journal Announcement: 9508W4

Abstract: By using an analog prefilter and a sampled data processor, it is possible to easily implement an entire class of weighting functions. Their main feature is a finite time duration; an additional interesting property is the small number of samples needed to process a pulse. Flat tops within better than 1% accuracy can also be achieved. Possible implementations of these filters are discussed with emphasis on causes of inaccuracy. In particular, these filters come out to be time-variant. Synchronization issues are therefore developed and thoroughly discussed. In a mixed analog-digital implementation, particular regard should be given to the A/D converter: the requirements on its characteristics are derived. (Author abstract) 4 Refs.

Descriptors: *Digital filters; Electric delay lines; Program processors; Synchronization; Analog to digital conversion; Sampled data control systems; Pulse shaping circuits

Identifiers: Sampled data processor; Analog prefilter; Finite time

duration; Analog to digital converter; Pulse pile-up; High quality analog delay line; Switched capacitor filter; Time limited pulse response
Classification Codes:
703.2 (Electric Filters); 703.1 (Electric Networks); 723.1 (Computer Programming); 723.2 (Data Processing); 731.1 (Control Systems); 713.5 (Other Electronic Circuits)
703 (Electric Circuits); 723 (Computer Software); 731 (Automatic Control Principles); 713 (Electronic Circuits)
70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS)

2/9/10 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03904624 E.I. No: EIP94071349700
Title: New class of weighting functions readily available with sampled data processors
Author: Ripamonti, G.; Castoldi, A.; Spigarolo, R.; Gatti, E.
Corporate Source: Universita degli Studi di Milano, Milano, Italy
Conference Title: Proceedings of the 1993 IEEE Nuclear Science Symposium & Medical Imaging Conference
Conference Location: San Francisco, CA, USA Conference Date: 19931030-19931106
Sponsor: IEEE
E.I. Conference No.: 20646
Source: IEEE Nuclear Science Symposium & Medical Imaging Conference pt 1 1994. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 630-634
Publication Year: 1994
CODEN: 001535 ISBN: 0-7803-1488-3
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 9409W2
Abstract: By using an analog prefilter and a sampled data processor, it is possible to easily implement an entire class of weighting functions. Their main feature is a finite time duration; an additional interesting property is the small number of samples needed to process a pulse. Flat tops within better than 1% accuracy can also be achieved. Possible implementations of these filters are discussed with emphasis on causes of inaccuracy. In particular, these filters come out to be time-variant. Synchronization issues are therefore developed and thoroughly discussed. In a mixed analog-digital implementation, particular regard should be given to the A/D converter: the requirements on its characteristics are derived. (Author abstract) 4 Refs.
Descriptors: *Digital filters; Electric delay lines; Program processors; Synchronization; Analog to digital conversion; Sampled data control systems ; Pulse shaping circuits
Identifiers: Sampled data processor; Analog prefilter; Finite time duration; Analog to digital converter; Pulse pile-up; High quality analog delay line; Switched capacitor filter; Time limited pulse response
Classification Codes:
703.2 (Electric Filters); 703.1 (Electric Networks); 723.1 (Computer Programming); 723.2 (Data Processing); 731.1 (Control Systems); 713.5 (Other Electronic Circuits)
703 (Electric Circuits); 723 (Computer Software); 731 (Automatic Control Principles); 713 (Electronic Circuits)
70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS)

2/9/11 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01948591 E.I. Monthly No: EI8602016185 E.I. Yearly No: EI86108995
Title: VOICE/DATA MULTIPLEXING IN A MULTI-SIGNAL PROCESSOR-SYNCHRONIZED ARCHITECTURE.
Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 5 Oct 1985 p 2059-2060
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8602
Abstract: The purpose of the proposed mechanism is to concentrate coded voice and data on the same high speed SDLC (Synchronous Data Link Control) agregate link. The digital output for each signal processor (SP) after running the concentration algorithm is N KBps including overhead. A voice activity detector (VAD) allows the non-transmission of the voice packets corresponding to the silence. The silence is artificially regenerated at the other end. During a conversation, the VAD detects silence during about 50% of the time.
Descriptors: *SIGNAL PROCESSING--*Digital Techniques; SPEECH--Processing; DATA PROCESSING--Multiplexing
Identifiers: VOICE/DATA MULTIPLEXING; PROCESSOR-SYNCHRONIZED ARCHITECTURE; CODED VOICE AND DATA; AGREGATE LINK; VOICE ACTIVITY DETECTOR (VAD)
Classification Codes:
716 (Radar, Radio & TV Electronic Equipment); 717 (Electro-Optical Communications); 718 (Telephone & Line Communications); 751 (Acoustics); 723 (Computer Software)
71 (ELECTRONICS & COMMUNICATIONS); 75 (ACOUSTICAL TECHNOLOGY); 72 (COMPUTERS & DATA PROCESSING)
?

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DATE: Monday, May 09, 2005

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		DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=OR	
☐	L32	L29 and (email or e-mail or (electronic adj1 mail))	24
☐	L31	L29 and (pda or (personal adj1 digital adj1 assistant))	11
☐	L30	L29 and (telephone near (system or directory or service))	2
☐	L29	(L26 or l27) and (convers$ or encrypt$ or crypt$)	55
☐	L28	(L26 or l27) and (synchron$ near (convers$ or encrypt$ or crypt$))	0
☐	L27	L25 and (synchroniz$ near (database$ or (data adj1 base$) or (data adj1 bank$) or databank$))	11
☐	L26	(l20 or l21 or l22 or l23 or l24 or l25) and (synchroniz$ near (cpu$ or computer$ or processor$ or terminal$))	118
☐	L25	709/230-231.ccls.	1368
☐	L24	709/203.ccls.	2646
☐	L23	707/201.ccls.	923
☐	L22	707/200.ccls.	1203
☐	L21	707/101.ccls.	1460
☐	L20	707/10.ccls.	3539
☐	L19	L17 and (database$ or (data adj1 base$) or (data adj1 bank$) or databank$)	5
☐	L18	L17 and (synchroniz$ near (database$ or (data adj1 base$) or (data adj1 bank$) or databank$))	0
☐	L17	L16 and (synchron$ near (convers$ or encrypt$ or crypt$))	25
☐	L16	(synchroniz$ near (cpu$ or computer$ or processor$ or terminal$))	5666
		DB=USPT; PLUR=NO; OP=OR	
☐	L15	L7 and (name or address or (phone adj1 number$))	17
☐	L14	L13 and (pda or (personal adj1 digital adj1 assistance))	55
☐	L13	(L11 or L12) and (databases or (data adj1 bases) or ((primary or host or first) near (database$ or (data adj1 base$))))	647
☐	L12	synchroniz$.ab.	25417
☐	L11	synchroniz$.ti.	8769
☐	L10	(L1 and L2) and (pda or (personal adj1 digital adj1 assistance))	1
☐	L9	L8 and (pda or (personal near digital near assistant))	1
☐	L8	6799190.pn.	1
☐	L7	(L3 or L4 or L5) and (telephone or call or calls)	20

10/693,175

☐	L6	(L3 or L4 or L5) and (pda or (personal near digital near assistant))	1
☐	L5	(L3 or L4) and (databases or (data adj1 bases) or ((primary or host or first) near (database$ or (data adj1 base$))))	16
☐	L4	(L1 or L2) and synchroniz$.ab.	29
☐	L3	(L1 or L2) and synchroniz$.ti.	16
☐	L2	(L1).pn. (5991390 6026439 6035246 6052688 6072891 6098058 6154751 6161145 6175842 6178510 3614737 3573730 3697984 3900797 3853010 3836768 3814841 3809814 3808373 4023753 4246638 4259720 4263649 4273962 4275449 4285039 4295039 4329191 4349196 4351023 4360875 4361851 4362928 4375101 4379497 4390953 4408291 4408203 4455453 4456972 4461028 4471163 4472626 4476381 4484273 4486828 4497066 4495851 4502038 4519069).pn. (4525859 4542808 4550402 4561105 4573196 4590468 4591823 4591705 4591704 4601011 4608631 4610206 4613979 4613965 4629164 4761543 4766418 4779198 4785563 4787033 4790118 4791675 4792899 4812627 4819154 4829445 4829451 4835711 4837568 4845744 4856066 4866756 4866771 4870419 4870683 4871085 4876717 4882474 4885779 4888638 4890098 4894857 4896273 4907268 4916611 4930604 4932022 4935635 4937581 4937742).pn. (4939672 4944827 4956770 4959855 4960982 4975969 4987587 4991087 4994969 4996714 4997144 5001710 5003317 5008930 5012522 5019976 5020105 5023868 5179701 5184314 5185727 5187790 5193114 5196846 5202828 5202921 5202929 5204663 5204961 5208756 5214269 5216672 5220511 5222062 5222152 5225976 5226040 5226080 5227967 5233510 5245329 5247161 5247575 5252953 5255183 5263157 5264828 5265033 5265238 5267314).pn. (5274714 5280586 5283733 5285383 5288980 5289183 5289369 5297283 5298725 5299134 5301275 RE34587 5307086 5309504 5311596 5319754 5321396 5321841 5325156 5325294 5337043 5341293 5343559 5353009 5354097 5361216 5363449 5364047 5365310 5375058 5381136 5387993 5388224 5392353 5400403 5404518 5408536 5412188 5414626 5418657 5418854 5420988 5420999 5422884 5432851 5446883 5450122 5465308 5467403 5469371).pn. (5469504 5469545 5471611 5473143 5473691 5475747 5481710 5488408 5490079 5491672 5497412 5497421 5507031 5509074 5511109 5511227 5513002 5513250 5513334 5515295 5515516 5517429 5519260 5519607 5521984 5523854 5524073 5526198 5530905 5533103 5534855 5535411 5539400 5544255 5546348 5548660 5550359 5553119 5555303 5557679 5560005 5561790 5568639 5576972 5579481 5581787 5586936 5594786 5598562 5604662).pn.	299
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END OF SEARCH HISTORY